A Comparative analysis of coding schemes in Low power baseband Transceiver IC for WBAN

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Abstract - In this paper, we present a low complexity ultra low power baseband transceiver IC for wireless body area network applications. Specified transceiver architecture for physical layer (PHY) is proposed and system performance is optimized. The Transceiver IC architecture is simulated in 0.12-μm CMOS technology, the baseband chip consumes 32.75 μW for TX mode and 37.15 μW for RX mode when working at a 250 kHz system clock, 1.1V supply and using LDPC code.

Index Terms—Digital circuit design, low power, wireless body area network (WBAN), wireless communication.

I. INTRODUCTION

The pursuit of higher quality of life motivates people to be more concerned about their health and potential diseases. At the same time, many patients can benefit from continuous monitoring of their diagnostic procedures. All these require a convenient healthcare surveillance system to monitor people’s health status anytime anywhere, especially when people suffer an acute event, such as a sudden heart attack. The tracking capability of such a system should also be able to provide optimal maintenance after a surgical procedure and support early detection of abnormal health conditions.

Recent advances in sensors, integrated circuits, and wireless communication are paving the way for developing miniature, lightweight, ultra-low power physiological healthcare surveillance and monitoring devices for the improvement of human lives. These devices can be integrated into wireless body area networks (WBANs) for health monitoring [1]. A WBAN topology consists of a series of miniature invasive/non-invasive physiological sensors and is able to communicate with other sensor nodes or with a central node [2]. The central node has higher computational capability and communicates wirelessly with a personal server and subsequently the outside world through a standard telecommunication infrastructure, such as wireless local area networks and cellular phone networks. Potential applications of WBANs include chronic disease management, medical diagnostics, home-monitoring, biometrics, and sports and fitness tracking, etc. [3], [4]. The power budget is quite strict for WBAN applications because the wireless device is powered by a battery.

Recently, transceivers for wireless personal area networks (WPANs) have been developed [5]–[7]. For example, the CC2420 from Texas Instruments in [5] can cover a 20–30 m range at a power consumption of 60~70 mW. However, such operation range and power consumption are not the optimal choice for WBAN applications, where the transceiver design target is a 1~3 m operation range to achieve ultra-low power. WBAN transceivers are proposed in [8]–[14]. Most of these transceivers have high data rate transmission, resulting in comparatively high power consumption. In [15], a low power low data rate digital baseband transceiver IC is proposed, which uses a low-complexity architecture to achieve satisfactory performance.

In this paper an optimized low power low data rate digital baseband IC is proposed, and its performance is analyzed in detail. The complete system requirements are illustrated in Table I. This chip is designed for low data rate and low power consumption. The working environment is the indoor WBAN application with 1~5 m working range. The specified raw data rate is 250 kb/s. The target power consumption is less than 50μW. Benefiting from the novel low complexity hardware architecture design and optimized hardware implementation, the proposed application specific integrated circuits (ASIC) can achieve lower power consumption as compared with [15]. A specified physical layer (PHY) architecture is developed, which reduces the complexity of baseband processing but maintains satisfactory performance.

In the following sections, we first present the proposed base-band transceiver architecture in Section II. In Section III, the important modules of the proposed baseband transceiver IC are introduced. Following that, the design implementation and measurement results are provided in Section IV. Finally, conclusions are drawn in Section V.
TABLE I
SYSTEM REQUIREMENT OF THE COMPLETE SYSTEM

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply</td>
<td>1.1v</td>
</tr>
<tr>
<td>Clock rate</td>
<td>4MHz</td>
</tr>
<tr>
<td>Working Range</td>
<td>1~5m</td>
</tr>
<tr>
<td>Raw data rate</td>
<td>250kbps</td>
</tr>
<tr>
<td>Target power consumption</td>
<td>&lt;50µw</td>
</tr>
</tbody>
</table>

Fig. 1. Block diagram of a complete WBAN radio transceiver.

II. PROPOSED LOW POWER BASEBAND TRANSCEIVER

The complete system diagram of a WBAN radio transceiver is shown in Fig. 1. In the transmitter block, the physical layer service data unit (PSDU) from the MAC layer is processed in the proposed transmitter (TX) baseband processor module to generate a physical layer protocol data unit (PPDU) packet. The channel coding and signal processing are performed on the PPDU in the TX baseband processor module, and the raw data rate of the TX baseband processor module output is 250 kb/s. The baseband raw data is modulated and then directly up-converted to a 2.45 GHz RF signal. In the receiver (RX) block, the received RF signal is down-converted to a 2 MHz intermediate frequency (IF) signal and then demodulated by a low power demodulator. The demodulated signal is processed by the proposed RX baseband processor module. Following that, the received PSDU is fed into the MAC layer. To achieve ultra low power consumption, a low-complexity PHY specification is proposed. The signal processing flow for TX and RX are presented in Figs. 2 and 3, respectively.

In the TX module, the baseband processor receives the PSDU from the MAC layer and constructs the PPDU. The permitted length of the PSDU within one packet should be no larger than 127 octets, and this information is contained in the PHY header (PHR) in octets. Once one packet of the PSDU is generated by the MAC layer, it is fed into TXFIFO and ready for transmission. There is a Prefix MUX block controlled by the TX state control block to select the input of the LDPC encoder block.

When a transmission command is sent from the MAC layer, the PHR is prefixed to the PSDU and sent into the LDPC encoder block first. The input data of the LDPC encoder block is in serial sequence with 1 bit word-length. In our design, (8, 4) LDPC coding and 8×4 matrix interleaving are used as forward error correction (FEC) coding. For each consecutive 4 bits of input data, the LDPC encoder block generates 8 bits of output data simultaneously, and thus the word-length of the LDPC encoder block output is 8 bits. The output data of the LDPC encoder block is fed into the 8×4 matrix interleaving block to suppress the burst error. To eliminate long strings of like bits that might impair receiver synchronization and to eliminate most periodic bit patterns that could produce undesirable frequency components (including the dc component), the interleaved data payload is first fed into a scrambling block and then coded by a Manchester encoder. The scrambling block generates the scrambling code in serial sequence with 1 bit word length. Here m sequence generator with m=4 as the scrambler to achieve satisfactory performance and comparatively low complexity. The output data of the interleaving block is in serial sequence with 1 bit word length and is XORed with the generated scrambling code. The scrambled data payload is fed into the Manchester encoder.

The Manchester encoder converts the bit “0” to bits “01” and converts the bit “1” to bits “10,” and thus the total number of “0” and “1” can be balanced. The output of the Manchester encoder is prefixed with the synchronization header (SHR) and is sent to the modulator for transmission.
In the receiver module, the received data stream is the demodulated binary signals from the demodulator. D flip-flop provided by the technology library to sample and to re-store the analog input. If the voltage of the input signal is higher than \( V_{\text{HL}} \) of the D flip-flop, the output of the D flip-flop will be \( "1.0\)". If the voltage of the input signal is lower than \( V_{\text{LH}} \) of the D flip-flop, the output of the D flip-flop will be \( "0.0\)". As illustrated in Fig. 3, the signals are first serially fed into the synchronization and data recovery (SDR) block to achieve synchronization and to recover the received data. The SDR block over-samples the incoming signal using a shift register matrix block and calculates the correlation between the incoming data and the predefined preamble sequence to achieve bit synchronization. The peak of the calculated correlation is continuously detected. Once the peak value is found, the start-of-frame delimiter (SFD) Correlator block calculates the correlations between the incoming data and the predefined SFD sequence, and the peak value is searched by the following peak detector block. Once the peak value is found, the packet synchronization is confirmed. The preamble sequence and SFD are removed and the Packet SYN block indicates to the RX State Control block that the PHR and PSDU can be received. The SDR block also generates the 250 kHz clock, and the RX State Control block selects the operation clock frequency of the RX baseband processor module which can be between 4 MHz clock and 250 kHz clock. Manchester decoding is first performed on the received PHR and PSDU data stream by detecting the first bit for every two continuous received bits. Following that, the incoming data is descrambled, and the structure of the descrambling block is identical to that of the scrambling block. The output of the descrambling block has a 1-bit word-length, and XOR operations are completed with the incoming data bit by bit. Following that, the PHR and PSDU are fed into the FEC decoding block, which includes the deinterleaving block and LDPC decoder block. The output of the deinterleaving block has an 8-bit word-length and is fed into the LDPC decoder block. The LDPC decoder block checks whether there is any error in the incoming data and corrects the error. If the LDPC decoder block detects an error but cannot correct it, the receiver will stop receiving any data and the MAC layer will request a retransmission of this packet. The PHR is decoded first and thus length information about the PSDU can be obtained by the RX state control block. The word-length of the LDPC decoder block output is 4 bits, and there is a parallel to serial buffer, so that bits in the PSDU are fed into the RX FIFO in serial sequence with 1 bit word-length, and is read by the MAC layer.

### III. MODULE DESIGN

In this section the block architectures for the PHY layer baseband will be presented briefly.

#### A. FIFO

FIFO is an acronym for First In, First Out, an abstraction related to ways of organizing and manipulation of data relative to time and prioritization. This expression describes the principle of a queue processing technique or servicing conflicting demands by ordering process by first-come, first-served (FCFS) behaviour: what comes in first is handled first, what comes in next waits until the first is finished, analogous to the behaviour of persons standing in line, where the persons leave the queue in the order they arrive, or waiting one’s turn at a traffic control signal. FIFOs are used commonly in electronic circuits for buffering and flow control which is from hardware to software. In hardware form a FIFO primarily consists of a set of read and write pointers, storage and control logic. Storage may be SRAM, flip-flops, latches or any other suitable form of storage. For FIFOs of non-trivial size a dual-port SRAM is usually used where one port is used for writing and the other is used for reading. An asynchronous FIFO is a FIFO where the same clock is used for both reading and writing. An asynchronous FIFO uses different clocks for reading and writing. Asynchronous FIFOs introduce metastability issues. A common implementation of an asynchronous FIFO uses a Gray code (or any unit distance code) for the read and writes pointers to ensure reliable flag generation. One further note concerning flag generation is that one must necessarily use pointer arithmetic to generate flags for asynchronous FIFO implementations. Conversely, one may use either "leaky bucket" approach or pointer arithmetic to generate flags in synchronous FIFO implementations.

#### B. Low Density Parity Check Codes

Low-density parity-check (LDPC) codes are class of linear block codes which provide near Shannon capacity performance. LDPC codes are mainly represented in two ways

(i) Matrix representation

(ii) Graphical representation
1) Matrix Representation

LDPC codes are class of linear block codes they can be described as certain $K$ dimensional subspace of $C$ of the vector space $\mathbb{F}^n$ 2 of binary $n$-tuples over the binary field $\mathbb{F}_2$. Hence the basis is expressed as $B = \{g_0, g_1, ..., g_{K-1}\}$, and this spans over $C$. Therefore each $c \in C$ can be expressed as $c = u_1 g_0 + u_2 g_1 + ... + u_{K-1} g_{K-1}$ for some $\{u_i\}$; thus $c = u g_c$, where $u=[u_0, u_1, ..., u_{K-1}]$. Here $G$ is the called the $k \times n$ generator matrix. The $(n-k)$ dimensional null space $C^\perp$ of $G$ comprises all vectors $x \in \mathbb{F}_2^n$ for which $x G^T = 0$ and is spanned by basis $B^\perp = \{h_0, h_1, ..., h_{N-K-1}\}$. Therefore $c H^T = 0$ where $H$ is known as the parity check matrix of dimension $(n-k) \times n$. Since it performs $m= n-k$ parity checks on the received codeword is called parity check matrix. The $H$ matrix for this code is represented as shown below

$$
H = \begin{pmatrix}
1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\
1 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 & 1 & 0 & 0 & 1 & 1 & 0 \\
0 & 0 & 1 & 0 & 0 & 1 & 0 & 1 & 0 & 1 \\
0 & 0 & 0 & 1 & 0 & 0 & 1 & 0 & 1 & 1 \\
\end{pmatrix}
$$

Fig. 4. Parity Check Matrix of a Linear Block Code.

2) Graphical Representation

LDPC codes are graphically represented using Tanner graphs. Tanner graphs also called as bipartite graphs of LDPC code is represented using nodes and connected by edges. There are two types of nodes
(i) Check nodes (cn)
(ii) Variable nodes (vn)

Check nodes (cn) represent the rows of the parity check matrix and the variable nodes (vn) represent the columns. The connection between the check nodes and variable nodes are determined by the elements of the $H$ matrix. Whenever the element $h_{ij}$ in the $H$ matrix is a 1, then there exits an edge between the check node $j$ and variable node $i$. The Tanner graph corresponding to the parity check matrix is shown in the above figure(5). In the above figure the variable nodes $v_0, v_1, v_2, v_3$ are connected to check node $c_0$, since in the $H$ matrix the elements $h_{00} = h_{01} = h_{02} = h_{03} = 1$. And similarly this hold good for all other check nodes.

There have been several major developments in the field of error correcting codes in the past and various coding techniques have been introduced, all of these techniques aim achieving reliable communication. Error correction is the ability to re-construct the original information which was transmitted. An error-correcting code is an algorithm for expressing a sequence of bits such that any errors which are introduced can be detected and corrected (within certain limitations) based on the remaining bits. In recent past the low density parity check codes (LDPC) gained more attention and is considered as the important error-correcting codes for the coming years in the field of telecommunication and magnetic storage.

C. Interleaver

Interleaving is frequently used in digital communication and storage systems to improve the performance of forward error correcting codes. Many communication channels are not memory less: errors typically occur in bursts rather than independently. If the number of errors within a code word exceeds the error-correcting code's capability, it fails to recover the original code word. Interleaving ameliorates this problem by shuffling source symbols across several code words, thereby creating a more uniform distribution of errors. The analysis of modern iterated codes, like turbo codes and LDPC codes, typically assumes an independent distribution of errors. Systems using LDPC codes therefore typically employ additional interleaving across the symbols within a code word. For turbo codes, an interleaver is an integral component and its proper design is crucial for good performance. The iterative decoding algorithm works best when there are not short cycles in the factor graph that represents the decoder; the interleaver is chosen to avoid short cycles. Interleaver designs include
(i) rectangular (or uniform) interleavers (similar to the method using skip factors described above)
(ii) convolutional interleavers
(iii) random interleavers (where the interleaver is a known random permutation)
(iv) S-random interleaver (where the interleaver is a known random permutation with the constraint that no input symbols within distance $S$ appear within a distance of $S$ in the output).

Another possible construction is a contention-free quadratic permutation polynomial (QPP). It is used for example in the 3GPP Long Term Evolution mobile
telecommunication standard. In multi-carrier communication systems, additional interleaving across carriers may be employed to mitigate the effects of prohibitive noise on a single or few specific carriers (e.g., frequency-selective fading in OFDM transmission).

D. Scrambler

A scrambler (also referred to as a randomizer) is a device that manipulates a data stream before transmitting. The manipulations are reversed by a descrambler at the receiving side. Scrambling is widely used in satellite, radio relay communications and PSTN modems. A scrambler can be placed just before a FEC coder, or it can be placed after the FEC, just before the modulation or line code. A scrambler in this context has nothing to do with encrypting, as the intent is not to render the message unintelligible, but to give the transmitted data useful engineering properties. A scrambler replaces sequences into other sequences without removing undesirable sequences, and as a result it changes the probability of occurrence of vexatious sequences. Clearly it is not foolproof as there are input sequences that yield all-zeros, all-ones, or other undesirable periodic output sequences.

A scrambler is therefore not a good substitute for a line code, which, through a coding step, removes unwanted sequences.

Purposes of scrambling
(i) It facilitates the work of a timing recovery circuit (see also Clock recovery), an automatic gain control and other adaptive circuits of the receiver (eliminating long sequences consisting of ‘0’ or ‘1’ only).
(ii) It eliminates the dependence of a signal’s power spectrum upon the actual transmitted data, making it more dispersed to meet maximum power spectral density requirements (because if the power is concentrated in a narrow frequency band, it can interfere with adjacent channels due to the cross modulation and the intermodulation caused by non-linearities of the receiving tract).

E. Manchester code

Manchester code (also known as Phase Encoding, or PE) is a line code in which the encoding of each data bit has at least one transition and occupies the same time. It therefore has no DC component, and is self-clocking, which means that it may be inductively or capacitively coupled, and that a clock signal can be recovered from the encoded data. Manchester code is widely used (e.g., in Ethernet; see also RFID or Near Field Communication). There are more complex codes, such as 8B/10B encoding, that use less bandwidth to achieve the same data rate but may be less tolerant of frequency errors and jitter in the transmitter and receiver reference clocks. Manchester code ensures frequent line voltage transitions, directly proportional to the clock rate; this helps clock recovery. The DC component of the encoded signal is not dependent on the data and therefore carries no information, allowing the signal to be conveyed conveniently by media (e.g., Ethernet) which usually do not convey a DC component.

Manchester code always has a transition at the middle of each bit period and may (depending on the information to be transmitted) have a transition at the start of the period also. The direction of the mid-bit transition indicates the data. Transitions at the period boundaries do not carry information. They exist only to place the signal in the correct state to allow the mid-bit transition. The existence of guaranteed transitions allows the signal to be self-clocking, and also allows the receiver to align correctly; the receiver can identify if it is misaligned by half a bit period, as there will no longer always be a transition during each bit period. The price of these benefits is a doubling of the bandwidth requirement compared to simpler NRZ coding schemes.

IV. DESIGN IMPLEMENTATION AND MEASUREMENT RESULTS

To achieve performance optimization and a short design period, the proposed baseband transceiver design requires a smooth and highly efficient design flow. VHDL RTL code is created to describe the PHY system and is verified on a Synopsys Design Compiler test platform.

| TABLE II | COMPARISON BETWEEN THE PROPOSED BASEBAND TRANSCEIVER AND CC2420 TRANSCEIVER |
|-----------------|-----------------|-----------------|-----------------|
| DESIGN          | POWER SUPPLY    | TRANSMITTER POWER | RECEIVER POWER  |
| The Proposed    | 1.1v            | 32.75µw          | 37.15µw         |
| CC 2420         | 3.3v            | 57.42mw          | 62.04mw         |
TABLE III
COMPARISON BETWEEN THE PROPOSED BASEBAND TRANSCEIVER AND EXISTING BASEBAND TRANSCEIVER

<table>
<thead>
<tr>
<th>ERROR CORRECTION CODES</th>
<th>TRANSCEIVER</th>
<th>INPUT POWER SUPPLY</th>
<th>POWER CONSUMPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>TRANSMITTER</td>
<td>1.1 Volt</td>
<td>32.7542(µw)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.2 Volt</td>
<td>39.0197(µw)</td>
</tr>
<tr>
<td></td>
<td>RECEIVER</td>
<td>1.1 Volt</td>
<td>37.1504(µw)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.2 Volt</td>
<td>45.2517(µw)</td>
</tr>
<tr>
<td>LDPC CODE</td>
<td>TRANSMITTER</td>
<td>1.1 Volt</td>
<td>34.5409(µw)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.2 Volt</td>
<td>42.2398(µw)</td>
</tr>
<tr>
<td></td>
<td>RECEIVER</td>
<td>1.1 Volt</td>
<td>39.4998(µw)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.2 Volt</td>
<td>47.6926(µw)</td>
</tr>
<tr>
<td>HAMMING CODE</td>
<td>TRANSMITTER</td>
<td>1.1 Volt</td>
<td>34.5409(µw)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.2 Volt</td>
<td>42.2398(µw)</td>
</tr>
<tr>
<td></td>
<td>RECEIVER</td>
<td>1.1 Volt</td>
<td>39.4998(µw)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.2 Volt</td>
<td>47.6926(µw)</td>
</tr>
</tbody>
</table>

From table 2, the design CC2420 from Texas instruments have default power consumption of 57.42 mW for transmitter and 62.04 mW for receiver. In the proposed design, the power consumption for transmitter is 32.75 µW and 37.15 µW for receiver. In table 3, the power consumption for the proposed work using LDPC code architecture and the existing hamming code architecture [15] for both transmitter and receiver are given. The results are obtained from Synopsys DC (Design Vision).

V. CONCLUSION

In this paper, low complexity baseband PHY transceiver architecture has been proposed. Based on the optimized system design, an ultra low power transceiver IC is realized in a 0.12-µm CMOS technology. For WBAN applications, it consumes only 32.75 µW for TX and 37.15 µW for RX at 250 kHz clock. This digital baseband chip can also be used for other communication baseband PHY processing with scalable data rate and power consumption.
REFERENCES


BIOGRAPHIES

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