450 mm Silicon Wafer:
Economical and Technical Challenges

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Abstract

Following Moore’s law semiconductor industry had acquired unprecedented growth by providing more capability at equal or low cost. Semiconductor industry increased the wafer size with new fab architecture at every ten years while technological and device advancements like miniaturization, new materials, silicon waste reduction, design and manufacturing process improvements at every two years which has reduced the cost per function. The capital investments require in overall factory integration has increased. This paper discusses the economical and technical issues regarding the transition to 450 mm. Technical challenges can be handled by making contemporary changes across semiconductor industry.

Keywords- 450 mm Wafer Diameter, fab economis, manufacturing process, wafer thickness.

I. INTRODUCTION

The present semiconductor fab industry is standardized on 300 mm diameter, as the device dimension is shrinking the cost of the chip is increasing this is counterbalance by increasing the diameter of the wafer. Thus, industries are planning to transit to 450 mm diameter wafer size, a wafer with large diameter makes it possible to produce more semiconductor devices from a single wafer [1]. Although timing is an important parameter it took industry 6 years to make transition from 150 mm to 200 mm, 10 years from 200 mm to 300 mm and similarly it will took for this transition. According to survey done in 2007 the expected arrival time is 2013 [2]. This transition will be supported by two factors, first, the rate at which silicon is consumed (millions of square inches of silicon per year) and second, the corresponding rate at which wafer capacity must be increased. Thus lower cost will give us new products, open new markets and extend business to new cost sensitive areas. In addition, this will enable efficient use of resources leading to reduce energy consumption. The economic situation has an impact on semiconductor industry which will affect this transition. The volume of silicon production is increasing with years Moore’s law hold an explanation to it. Economic statement of law says that evolution of technology brings more components and thus giving greater functionality for the same cost, computing power improves, driving productivity in the economy thus fueling demand for more semiconductors. Moore’s law worked because of reduction in feature size, increased yield, and increased package density.

![Figure 1: Volume of silicon wafer consumption](image-url)
II. ECONOMICS OF 450 mm WAFERS

For next generation large wafer diameter the reduction in cost would be observed if there is no increment in wafer and device production equipment. Since larger wafer area requires more capital investment in factory equipments and for same yield the production throughput does not decrease. The quote by Goodal et al [3] "When the wafer area increases by >2 times, but the cost of the new tool set for the same number of wafer starts increases by only 30-40% (which is typical), the cost per area decreases by 30-50%; an annualized improvement of ~4% when wafer size changes occur about every 10 years, Thus semiconductor industries realized that an increase in wafer diameter gives a phenomenal, 30-50%, decrease in unit area cost therefore it is necessary for them to make investments in larger-diameter plant capacity. The verification of this model on 450 mm is ambiguous. The assumption been made in the economic model that the cost per square inch of the silicon wafer remains the same (or in fact declines) as the wafer sizes increase this has created differences between the actual cost of the silicon wafer manufacturing process and the actual cost of wafer. As the wafer diameter increases cost is affected by number of factors such as the cost of single crystal depends on crystal growth conditions which is slower in comparison to 300 mm, pull rates must be reduced, utilization efficiency of poly-silicon starting charge is renew, cost of pullers and associated factory utilization to be increase, cost of wafer depends on wafer shaping and wafer thickness which increases with diameter. For a silicon wafer manufacturing industry, there is no sufficient economic incentive at all levels of the supply chain, to invest in the development of 450 mm substrate [4]. The semiconductor industry in present condition is not able to move to larger diameter wafer because there is negligible help form the rest of the industry in funding the development and transition and following of the assumption that cost per square inch does not increase.

III. TECHNICAL CHALLENGES

In order to realize 450 mm silicon crystal growth having weight 800 kg and length of 215 cm, many technological challenges had to be overcome. Some of them are listed [5].

1. Development of a new mechanism to replace the use of the 'Dash' neck to suspend very heavy crystals. Weight of crystal is expected to be around a ton.
2. The growth times of crystal is very large this increases the risk of dislocations in the crystals.
3. Development of quartz crucibles of 900 mm and larger with improved quality, so that it can withstand large manufacturing times.
5. Establishment of safety precautions to prevent steam explosions caused by leakage of heavily charged silicon melt more than 600 kg.

The CZ method is the most preferred method for growing crystals of semiconductor; it involves growing a neck, a crown, the body of the crystal and then a tail or end-cone. The method involves melting the raw material in crucible, a seed crystal is placed in contact with the top, cooler region of the melt is rotated slowly and gradually pulled upwards. The 450 mm crystals are so big (215 cm) and heavy that they have many challenging issues. The dash neck technique required to grow a dislocation free crystals works very well with less diameter wafer. Dash neck which is few millimeters in diameter will support whole of the crystal no matter how heavy the crystal ingot. In 450 mm the dash neck is not able to sustain the whole crystal so a new two step growth technique is introduced. In first step A Dash neck was first grown to eliminate dislocations after this a second suspending cone was grown to support the heavy crystal weight by the other mechanics. In order to held the cone and sustained the weight of the crystal body tool called a clamp or tray is used.

A. Material Losses

To achieve properly distributed finished wafer diameter the body is grown slightly more than the diameter this extra peripheral material is removed by accurately grinding to the required diameter. The shaded areas in Figure 3 show the silicon removed during these initial cutting and shaping.
processes and which contribute to the crystal yield losses, since it has large size more material loss occurs.

B. Kerf Losses

All silicon ingots are sawn into wafers by wire saws which are usually silicon carbide particles carried by thin iron wire in presence of a cutting fluid this generates a large amount of micron size powder waste termed as ‘kerf’ [3] the amount is depended on the diameter more is the diameter more is the loss. There are two basic solutions to the above problem either the effects of the sawing process should be virtually eliminated by the direct growth of the substrates or if the present sawing process is continued the waste powdered ‘kerf’ should be recovered and recycled into the process.

Any kerf recycling process has to deal with the issues of separation, purification and compaction, especially if the powder is to be recycled as feedstock into the microelectronics industries.

C. Wafer Shaping

Wafer shaping is to prepare the wafer for devices fabrication by removing any residual mechanical damage the wafers are mechanically lapped in a Slurry of alumina and glycerin then etching is performed. Then one or both is polished by electrochemical process. The volume of removals in 450 mm will be the twice of 300 mm. Shape is of extreme importance especially flatness, will be a key issue. The downstream processing will require larger machines, Thermal processing for epi, annealing and similar steps will require significant work.

D. Wafer Thickness

The scaling of wafer thickness in accordance with the diameter is dependent on number of factors Such as gravitational sag, Warpage, vibration and displacement during transport

E. Wafer Scaling(Empirically)

The thickness of wafer increases with the diameter of wafer since thin film is hard to handle because of their fragility, with the help of extrapolation method in the plot gives the diameter of about 800 μm [6].

F. Effect Gravitational Sag

Sagging is an important factor in wafer thickness scaling. During wafer shaping and device fabrication it is necessary to keep wafer straight but because of the weight of the wafer a bend is produced [6].

\[
\delta = \frac{kR^4}{D}
\]

\[
D = \frac{Et^3}{12(1-\nu)}
\]
Where $R$ is wafer radius, $E$ is Young’s modulus, $\nu$ is Poisson ratio, $t$ is thickness, and scaling factor is $R^4/t^3$. To have the same tolerance of wafer sag as a 300 mm wafer (thickness: 775µm), a 450 mm wafer would need to have a thickness of 1,800µm (1.8mm) [7].

G. Warpage

Warp occurs because of the difference between the lattice constant of the substrate wafer and the epitaxial layer.

Epitaxial wafers are expected to continue to be used at the 450 mm diameter. These are high quality wafers consisting of a single crystal silicon vapor phase layer several microns thick (epitaxial layer) grown on the surface of a substrate wafer.

The wafer thickness of at least 1,020 µm would be required for a 2 µm epitaxial layer. A wafer thickness of at least 1,430 µm would be needed for a 4 µm epitaxial layer.

IV. CONCLUSIONS

The roadmap towards production of 450 mm wafers is taking shape; Intel and TSMC have begun their transition at the beginning of this year. But the large cost involved in developing the infrastructure and prevailing of the misconception among vendors that this transition would be of no benefit had delayed this transition. Manufacturing of 450 mm crystals will require innovation in terms of both manufacturing factory equipment and manufacturing processes.
REFERENCES


